500.35578CC5

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: K. OSADA, et al.

Application No.: Rule 1.53(b) Continuation of U.S. Patent Application

Serial No. 10/320,516, filed December 17, 2002

Filed: On even date herewith

For: SEMICONDUCTOR MEMORY APPARATUS,

SEMICONDUCTOR APPARATUS, DATA PROCESSING

APPARATUS AND COMPUTER SYSTEM

Art Group of Parent: 2818

Examiner of Parent: H. V. Ho

## <u>INFORMATION DISCLOSURE STATEMENT</u> <u>UNDER 37 CFR §1.97 & 1.98</u>

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 October 17, 2003

Sir:

In the matter of the above-identified application, this Information Disclosure Statement is being submitted with the following citation as specified in 37 CFR §1.97(d).

"A copy of any patent, publication or other information listed in an Information Disclosure Statement is not required to be provided if it was previously cited by or submitted to the Office in a prior application, provided that the prior application is properly identified in the statement and relied upon for an earlier filing date under 35 U.S.C. §120."

Applicants are submitting herewith a copy of Form PTO/SB/08A which list documents cited in parent applications Serial No. 10/320,516, filed December 12, 2002, which is a continuation of application Serial No. 09/988,197, filed November 19, 2001; which is a continuation of application Serial No. 09/577,149, filed May 24,

2000 (now USP 6,396,732); which is a continuation of application Serial No. 08/906,883, filed August 6, 1997 (now USP 6,091,629), the entire disclosures of which are hereby incorporated by reference.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (500.35578CC5).

Respectfully submitted,

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Approved for use through 10/31/2002. OMB 0651-0031

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C	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Examiner Initials'		Number-Kind Code <sup>2</sup> (if known)			
		5.253.207	10/93	Shikatani	
		5.675.529	10/97	Poole	
		5.574.687	11/96	Nakase	
		5.517.462	05/96	lwamoto et al	
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Initials'	No. <sup>1</sup>	Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)	MM-DD-YYYY	Applicant of Cited Document	or Relevant Figures Appear	T <sup>6</sup>
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		2-50396	2/90			
		7-201197	8/95			

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where outlished			
·		Osada et al., "A 2ns Access, 285MHz, Two-Port Cache Macro Using Double Global Bit-Line Pairs" ISSCC Digest of Technical Papers, pp. 402-403			
		Kushiyami et al., "A 295MHz CMOS 1M (x256) Embedded SRAM Using Bi-directional Read/Write Shared Sense Amps and Self-Timed Pulsed Word-Line Drivers" ISSCC Digest of Technical Papers, Feb. 1995, pp. 304-305			
		IEEE Journal of Solid State Circuits, Vol. 23, No. 5, Oct. 1988, pp. 1048-1053			

Examiner	Date	
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